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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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HARNESS, DICKEY & PIERCE, P.L.C.
P.O. BOX 8910
RESTON, VA 20195

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/763,164	LEE, CHAN-SUK	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/763164 Attorney's Docket #: 2557-000200/US
Filing Date: 1/26/2004; claimed foreign priority to 2/20/2003

Applicant: Lee

Examiner: Alexander Williams

Applicant's Amendment filed 9/28/05 has been acknowledged.

Claims 1 to 19 and 21 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 16, 21, 22 and throughout, Applicant claims conductors and can claim as broadly as desired. Conductors can be anything that conducts electricity. Was is the intent or is the conductive element missing? For example, "conductor wires"?

In claims 1, 16 and 21, the phrase "the frame" lack proper antecedent basis. There is no previously mentioned "frame" in the claims.

In claim 4, "a frame" is claimed. Is this the same frame in claim one now?

In claim 16, it is unclear and confusing to what is meant by and how "a number, **n**, of **intermediate semiconductor chips** wherein **n is an integer** greater than or **equal to 0**; each intermediate semiconductor chip being stacked offset over **a semiconductor chip (Is this a different semiconductor chip from already described?)** located underneath the intermediate semiconductor chip such that a portion of the semiconductor chip underneath is exposed; a second semiconductor chip stacked offset over the intermediate semiconductor chips or the first semiconductor chip such that **a portion of the topmost intermediate semiconductor chip is exposed;.....at least one first conductor** electrically **connecting** the exposed portions of the first and **intermediate semiconductor chips** to the second semiconductor chip" can happen when n is zero, "0"? When n is zero, the portion of the topmost

intermediate semiconductor chip being exposed does not even exist. When n is zero, how is this possible when you would only have first and second semiconductor chips and **no intermediate semiconductor chips**? When n is zero, the at least one conductor cannot be connected to the intermediate semiconductor chip because is not a intermediate semiconductor chip.

Any of claims 1 to 19 and 21 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, 6, 7, 16, 17, 19 and 21, **insofar as they can be understood**, are rejected under 35 U.S.C. § 102(e) as being anticipated by Haba et al. (U.S. Patent # 6,376,904 B1).

1. Haba et al. (figures 1 to 14) specifically figure 13 show a stacked semiconductor package **1300** comprising: a first semiconductor chip **(1312,1314)**; a second semiconductor chip **((lower bottom chip under 1312,1314 but not labeled)** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; at least one first conductor **(wire electrically connecting 1312 to lower bottom chip under 1312 but not labeled)** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **(conductor wires and electrode pad electrically extending from the lower bottom chip under 1312 but not labeled electrically connecting to the pad on 420)** electrically connecting the second semiconductor chip to the frame **420**.

2. The package of claim 1, Haba et al. show wherein the first conductor electrically connects at least one bond pad **(pad on 1312 but not labeled)** on the first semiconductor chip with at least one bond pad **(pad on lower bottom chip under 1312 but not labeled)** on the second semiconductor chip.

6. The package of claim 1, Haba et al. show wherein a plurality of first conductors **(wire and pad, since pads are conductors or (wire electrically connecting 1312 to lower bottom chip under 1312 but not labeled) and 1310 connected to 1314 on the 1312,1314 chip)** electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Haba et al. further comprising: the plurality of first conductors **(11,10**

and bond pad on bottom of first chip 1314,1312) respectively electrically connecting a plurality of bond pads on the first semiconductor chip to a first plurality of bond pads on the second semiconductor chip.

16. Haba et al. (figures 1 to 14) specifically figure 13 show a stacked semiconductor package **1300** comprising: a first semiconductor chip **(chip 1312,1314)**; a number, n, of intermediate semiconductor chips **(bottom chip under chip 1312,1314)** wherein n is an integer greater than or equal to 0; each intermediate semiconductor chip being stacked offset over a semiconductor chip located underneath the intermediate semiconductor chip such that a portion of the semiconductor chip underneath is exposed; a second semiconductor chip **(second bottom chip under chip 1312,1314)** stacked offset over the intermediate semiconductor chips or the first semiconductor chip such that a portion of the topmost intermediate semiconductor chip is exposed; at least one first conductor **(wire connecting the bottom two chips under chip 1312,1314)**electrically connecting the exposed portions of the first and intermediate semiconductor chips to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **(wire connecting the seconds chip under chip 1312,1314 connecting to 420)** electrically connecting the second semiconductor chip to the frame **420**.

17. The package of claim 16, Haba et al. show wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first, second and third semiconductor chips to a first plurality of bonding pads on the fourth semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

19. The package of claim 1, Haba et al. show wherein the first and second semiconductor chips are a same type of chip.

21. Haba et al. (figures 1 to 14) specifically figure 13 show a method for fabricating a stacked semiconductor package **1300**, comprising: forming a stacked chip package including at least a first semiconductor chip **1312,1314** and a second semiconductor chip **(one of the clips under chip 1312,1314)** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor **(the wire connect chip 1312 to the lower two chips but not labeled)** such that the conductor does not extend beyond a periphery of the first semiconductor chip; and electrically connecting the second semiconductor chip to the frame **420**.

Claims 1, 2, 6-8, 16, 17, 19 and 21 are rejected under 35 U.S.C. § 102(e) as being anticipated by Verma et al. (U.S. Patent Application Publication # 2003/0155659 A1).

1. Verma et al. (figures 1 to 14) specifically figure 6 show a stacked semiconductor package **60** comprising: a first semiconductor chip **40b**; a second semiconductor chip **40a** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; at least one first conductor **68** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **69** electrically connecting the second semiconductor chip to the frame **62**.

2. The package of claim 1, Verma et al. show wherein the first conductor electrically connects at least one bond pad (shown, but not labeled) on the first semiconductor chip with at least one bond pad (shown, but not labeled) on the second semiconductor chip.

6. The package of claim 1, Verma et al. show wherein a plurality of first conductors **68** electrically connect the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Verma et al. further comprising: the plurality of first conductors **68** respectively electrically connecting a plurality of bond pads (shown but not labeled) on the first semiconductor chip to a first plurality of bond pads (shown but not labeled) on the second semiconductor chip.

8. The package of claim 7, Verma et al. show wherein the plurality of bonds pads on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second semiconductor chip corresponding to the edge of the first semiconductor chip.

16. Verma et al. (figures 1 to 14) specifically figure 6 show a stacked semiconductor package **60** comprising: a first semiconductor chip **40b**; a number, n, of intermediate semiconductor chips **(N is 0 so not needed)** wherein n is an integer greater than or equal to 0; each intermediate semiconductor chip being stacked offset over a semiconductor chip located underneath the intermediate semiconductor chip such that a portion of

the semiconductor chip underneath is exposed; a second semiconductor chip **40a** stacked offset over the intermediate semiconductor chips or the first semiconductor chip such that a portion of the topmost intermediate semiconductor chip is exposed; at least one first conductor **68** electrically connecting the exposed portions of the first and intermediate semiconductor chips to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **69** electrically connecting the second semiconductor chip to the frame **62**.

17. The package of claim 16, Verma et al. show wherein a plurality of first conductors electrically connect bonding pads on the exposed portions of the first, second and third semiconductor chips to a first plurality of bonding pads on the fourth semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

19. The package of claim 1, Verma et al. show wherein the first and second semiconductor chips are a same type of chip.

21. Verma et al. (figures 1 to 14) specifically figure 6 show a method for fabricating a stacked semiconductor package **60**, comprising: forming a stacked chip package including at least a first semiconductor chip **40b** and a second semiconductor chip **40a** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor **68** such that the conductor does not extend beyond a periphery of the first semiconductor chip; and electrically connecting the second semiconductor chip to the frame **62**.

Claims 1 to 22, **insofar as some of them can be understood,** are rejected under 35 U.S.C. § 102(e) as being anticipated by Kato et al. (U.S. Patent Application Publication # 2002/0140107 A1).

1. Kato et al. (figures 1 to 35) specifically figures 1 and 2 show a stacked semiconductor package **10A** comprising: a first semiconductor chip **11a**; a second semiconductor chip **12a** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; at least one first conductor **14** electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **15** electrically connecting the second semiconductor chip to the frame **13**.

2. The package of claim 1, Kato et al. show wherein the first conductor electrically connects at least one bond pad **19** on the first semiconductor chip with at least one bond pad **18** on the second semiconductor chip.

3. The package of claim 2, Kato et al. further comprising: a redistribution pattern **51** electrically connecting the bond pad on the second semiconductor chip to a differently positioned bond pad on the second semiconductor chip (figures 14 and 15).

4. The package of claim 3, Kato et al. further comprising: a frame **13** supporting a chip package structure, the chip package structure including at least the first and second semiconductor chips; and at least one second conductor **15** electrically connecting the differently positioned bond pad to the frame.

5. The package of claim 4, Kato et al. show wherein the second conductor **15** electrically connects the differently positioned bond pad **18A,18B** to a bond pad on the frame (figures 14 and 15).

6. The package of claim 1, Kato et al. show wherein a plurality of first conductors **14** electrically connect

the exposed portion of the first semiconductor chip to the second semiconductor chip, the plurality of first conductors not extending beyond a periphery of the first semiconductor chip.

7. The package of claim 6, Kato et al. further comprising: the plurality of first conductors **14** respectively electrically connecting a plurality of bond pads **19** on the first semiconductor chip to a first plurality of bond pads **18** on the second semiconductor chip.

8. The package of claim 7, Kato et al. show wherein the plurality of bonds pads **19** on the first semiconductor chip are arranged adjacent to an edge of the first semiconductor chip, and the first plurality of bond pads **18** on the second semiconductor chip are arranged adjacent to an edge of the second semiconductor chip, the edge of the second semiconductor chip corresponding to the edge of the first semiconductor chip.

9. The package of claim 8, Kato et al. further comprising: a redistribution pattern **51** electrically connecting the first plurality of bond pads **18A,18B** on the second semiconductor chip to a second plurality of bond pads on the second semiconductor chip, the second plurality of bond pads arranged adjacent to a different edge of the second semiconductor chip (see figures 14 and 15).

10. The package of claim 7, Kato et al. further comprising: a redistribution pattern **51** electrically connecting the first plurality of bond pads **18B** on the second semiconductor chip to a second plurality of bond pads **18A** on the second semiconductor chip (see figures 14 and 15).

11. The package of claim 10, Kato et al. further comprising: a frame **13** supporting a chip package structure, the chip package structure including at least the first **11A** and second **12A** semiconductor chips; and a plurality of second conductors **15**

electrically connecting the second plurality of bond pads on the second semiconductor chip to the frame (see figures 14 and 15).

12. The package of claim 11, Kato et al. show wherein the frame **13** is one of a printed circuit board and a flexible substrate.

13. The package of claim 11, Kato et al. show wherein the frame includes a die pad portion supporting the chip package structure and an inner lead portion to which the plurality of second conductors are electrically connected (see paragraph [0013]).

14. The package of claim 13, Kato et al. further comprising: a sealing resin **16** sealing the first and second semiconductor chips, the redistribution pattern, the first and second plurality of conductors, and a portion of the frame see paragraph [0013]).

15. The package of claim 11, Kato et al. show wherein the plurality of first and second conductors **14,15** are bonding wires.

16. Kato et al. (figures 1 to 35) specifically figure 34 show a stacked semiconductor package **10J** comprising: a first semiconductor chip **30C**; a number, n, of intermediate semiconductor chips **31C** wherein n is an integer greater than or equal to 0; each intermediate semiconductor chip being stacked offset over a semiconductor chip located underneath the intermediate semiconductor chip such that a portion of the semiconductor chip underneath is exposed; a second semiconductor chip **12I** stacked offset over the intermediate semiconductor chips or the first semiconductor chip such that a portion of the topmost intermediate semiconductor chip is exposed; at least one first conductor **14** electrically connecting the exposed portions of the first and intermediate semiconductor chips to the second semiconductor chip, the first conductor not extending beyond a periphery of the first semiconductor chip; and at least one second conductor **15** electrically connecting the second semiconductor chip to the frame **13**.

17. The package of claim 16, Kato et al. show wherein a plurality of first conductors **14** electrically connect bonding pads **19** on the exposed portions of the first and intermediate semiconductor chips to a first plurality of bonding pads **18** on the second semiconductor chip, the first conductors not extending beyond a periphery of the first semiconductor chip.

18. The package of claim 17, Kato et al. further comprising: a redistribution pattern **51** electrically connecting the first plurality of bond pads **18B** on the second semiconductor chip **12A** to a second plurality of bond pads **18A** on the second semiconductor chip (see figures 14 and 15).

19. The package of claim 1, Kato et al. show wherein the first and second semiconductor chips are a same type of chip.

20. Kato et al. (figures 1 to 35) specifically figures 14 and 15 show a stacked semiconductor package **10E** comprising: a stacked chip structure including an upper semiconductor chip **12A** and at least one lower semiconductor chip **11A** disposed under at least a portion of the upper semiconductor chip; and a redistribution pattern **51** redistributing a first plurality of bond pads **18A** on the upper semiconductor chip to a differently positioned second plurality of bond pads **18B** on the upper semiconductor chip, the first plurality of bond pads **18A** being electrically connected with the lower semiconductor chip **11A**.

21. Kato et al. (figures 1 to 35) specifically figures 1 and 2 show a method for fabricating a stacked semiconductor package **10A**, comprising: forming a stacked chip package including at least a first semiconductor chip **11A** and a second semiconductor chip **412A** stacked offset over the first semiconductor chip such that a portion of the first semiconductor chip is exposed; electrically connecting the exposed portion of the first semiconductor chip to the second semiconductor chip using at least one conductor **14** such that the conductor does not extend beyond a periphery of the first semiconductor chip; and electrically

connecting the second semiconductor chip to the frame **13**.

22. Kato et al. (figures 1 to 35) specifically figures 14 and 15 show a method for fabricating a stacked semiconductor package **10E**, comprising: forming a stacked chip structure including an upper semiconductor chip **12A** and at least one lower semiconductor chip **11A** disposed under at least a portion of the upper semiconductor chip; and electrically connecting the lower semiconductor chip with a first plurality of bond pads **18A** on the upper semiconductor chip; and forming a redistribution pattern **51** redistributing the first plurality of bond pads **18B** on the upper semiconductor chip to a differently positioned second plurality of bond pads **18B** on the upper semiconductor chip.

Response

Applicant's arguments filed 9/28/05 have been fully considered, but are moot in view of the new and modified grounds of rejections detailed above.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/686,685,723,777,784,786,787,773,696,698	6/24/05 11/5/05
Other Documentation: foreign patents and literature in 257/686,685,723,777,784,786,787,773,696,698	6/24/05 11/5/05
Electronic data base(s): U.S. Patents EAST	6/24/05 11/5/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
11/5/05